# Optimizing Gallium Nitride (GaN) Based Inverters for Next-Generation Electric Vehicle Fast-Charging Stations

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Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are rapidly emerging as the enabling technology for next-generation electric vehicle (EV) fast-charging stations, offering superior switching performance over conventional silicon-based devices. This paper investigates the optimisation of GaN-based two-stage inverter architectures — comprising a totem-pole bridgeless power factor correction (PFC) front-end and an LLC resonant DC-DC stage — for high-power EV fast-charging applications. Key optimisation parameters including switching frequency selection, dead-time minimisation, zero-voltage switching (ZVS) range extension, and thermal management strategies are systematically analysed. The comparative performance of GaN against silicon carbide (SiC) and silicon (Si) devices is evaluated across efficiency, power density, and electromagnetic interference (EMI) dimensions. Results indicate that GaN-based inverters can achieve power conversion efficiencies exceeding 98% at switching frequencies of 100-500 kHz, with passive component volume reductions of 30-60% relative to Si baselines. Implementation challenges including dynamic on-resistance degradation, gate-driver design complexity, and high-frequency EMI compliance are critically examined. The paper concludes with a topology-selection framework and a research roadmap for GaN deployment in 400 V and 800 V EV charging architectures.

**Keywords:** *GaN HEMT; EV fast charging; totem-pole PFC; LLC resonant converter; wide bandgap semiconductor; power density; zero-voltage switching*

## 1. Introduction

The global transition towards electrified transportation has intensified demand for fast, reliable, and energy-efficient electric vehicle (EV) charging infrastructure. Conventional silicon (Si) insulated-gate bipolar transistors (IGBTs) and MOSFETs, which have dominated power electronics for decades, are approaching fundamental material limits in switching frequency, power density, and thermal performance that constrain the achievable performance of EV charging inverters [1]. Wide-bandgap (WBG) semiconductors — principally silicon carbide (SiC) and gallium nitride (GaN) — have emerged as enabling alternatives, with material properties that unlock substantially higher switching frequencies, lower on-resistance, and superior thermal characteristics [2].

GaN high-electron-mobility transistors (HEMTs) are characterised by a bandgap of 3.4 eV, a critical electric field of approximately 3.3 MV/cm, and near-zero reverse recovery charge attributable to the absence of a parasitic body diode. These properties enable GaN devices to operate at switching frequencies an order of magnitude above Si IGBTs — from 100 kHz to beyond 1 MHz — while maintaining competitive conduction losses at voltage ratings up to 650 V. The consequent reduction in passive component size translates directly into higher inverter power density, a critical metric for on-board and off-board EV charging equipment where volume and weight are constrained [3].

EV fast-charging stations operating at power levels of 50-350 kW require inverter architectures capable of high power factor rectification, isolated DC-DC conversion, and compatibility with both 400 V and 800 V vehicle battery architectures. The totem-pole bridgeless PFC and the LLC resonant DC-DC converter have emerged as preferred topologies for GaN-based implementations due to their inherent soft-switching characteristics and high-efficiency profiles [4]. However, realising the theoretical performance potential of GaN in these topologies requires careful optimisation of switching parameters, gate-driver design, and thermal management strategies that differ substantially from established Si practice [5].

This paper presents a systematic optimisation analysis of GaN-based two-stage inverter architectures for EV fast-charging applications. The principal contributions are: (i) a comparative evaluation of GaN against SiC and Si devices across efficiency, power density, and EMI dimensions; (ii) an optimisation framework for switching frequency, dead time, and ZVS range in totem-pole PFC and LLC converter stages; (iii) a thermal management analysis addressing GaN-specific challenges including dynamic on-resistance and junction temperature constraints; and (iv) a topology-selection framework for 400 V and 800 V charging architectures. The remainder of the paper is structured as follows. Section 2 reviews the relevant literature. Section 3 describes the optimisation methodology. Section 4 presents results and discussion. Section 5 addresses implementation challenges. Section 6 concludes with future research directions.

## 2. Literature Review

The fundamental material properties of GaN that confer its power electronics advantage are well established. The two-dimensional electron gas (2DEG) formed at the AlGaN/GaN heterojunction yields high electron mobility exceeding 2000 $cm^2/V \cdot s$, enabling low on-resistance in lateral HEMT structures while supporting breakdown voltages of 600-900 V suitable for EV charging applications. Chen et al. [6] provided a comprehensive review of GaN-on-Si power technology, documenting the device physics, material growth, and application landscape that underpins commercial 650 V GaN platforms.

A systematic comparison of GaN and SiC device technologies for EV applications, conducted by Buffolo et al. [7], established that GaN exhibits clear advantages in mid-power soft-switched converters operating at voltages up to 650 V, while SiC MOSFETs maintain dominance in high-voltage (900-1200 V) traction inverter applications. For 400 V bus architectures — the current mainstream for passenger EVs — GaN emerges as the preferred switch for on-board charger (OBC) applications where switching frequencies above 100 kHz are beneficial for passive size reduction. Iannaccone et al. [8] examined the broader landscape of WBG semiconductor

opportunities and challenges, identifying EMI and gate-driver complexity as the principal barriers to GaN adoption in power conversion.

The bridgeless totem-pole PFC converter is particularly well suited to GaN implementation because its continuous conduction mode (CCM) operation requires switches with negligible reverse recovery — a condition GaN HEMTs satisfy but Si MOSFETs body diodes do not. Liu et al. [9] demonstrated a GaN-based MHz totem-pole PFC rectifier achieving 99% efficiency at 1 MHz switching frequency, establishing the viability of high-frequency CCM PFC with GaN. Subsequent work by Soares et al. [10] reported a high-efficiency interleaved totem-pole PFC converter with voltage-follower characteristics achieving 98.9% peak efficiency at the 6.6 kW power level relevant to Level 2 OBC applications.

The advantages of interleaved operation for current ripple cancellation and passive reduction were quantified in a 7.2 kW design study targeting OBC applications [11], which confirmed that two-phase interleaving at 50 kHz in CCM allows a 60% reduction in PFC inductor size relative to single-phase designs while maintaining total harmonic distortion (THD) below the IEC 61000-3-2 Class A limit. For 800 V bus architectures, three-level Vienna or T-type rectifier configurations exploiting 650 V GaN devices in series-stacked arrangements have been identified as promising alternatives that avoid the need for 900 V-rated devices [3].

The LLC resonant converter is the dominant DC-DC stage topology for isolated EV charger applications due to its wide soft-switching range, high efficiency, and low EMI profile. Mudiyanselage et al. [12] provided a comprehensive review of DC-DC resonant converter topologies and control techniques for EV applications, identifying dead-time optimisation and adaptive frequency modulation as key levers for efficiency improvement in GaN-based implementations. The transition to GaN devices in LLC stages enables switching frequencies above 500 kHz, which reduces transformer and resonant inductor volumes substantially but introduces stringent requirements on gate timing and parasitic inductance management.

Zhang et al. [13] conducted a detailed analysis of dead-time energy loss in GaN-based triangular current mode (TCM) converters, demonstrating that excessive dead time at light loads is a primary contributor to efficiency degradation in GaN LLC stages. An adaptive dead-time strategy, wherein the gate-turn-on event is triggered by dv/dt detection to confirm zero-voltage conditions prior to switch activation, was shown to recover 0.5-1.2% efficiency at partial loads. Elezab et al. [14] reported a high-efficiency LLC resonant converter with output range 200-1000 V targeting DC-connected ultra-fast charging stations, achieving 97.6% peak efficiency in a GaN-based full-bridge implementation.

Thermal management represents a critical constraint on GaN HEMT power density, arising from the device's lateral structure, which concentrates power dissipation in a narrow channel region, and from the elevated thermal boundary resistance at GaN/substrate interfaces. Malakoutian et al. [15] investigated the integration of near-junction diamond heat spreaders with GaN HEMT devices, demonstrating a factor-of-three increase in allowable power density through thermal pathway engineering. For system-level applications, Lumbreras et al. [16] examined the effect of heat dissipation system design on hard-switching GaN converter performance, quantifying the impact of substrate thermal conductivity on maximum allowable switching frequency and power density.

A further GaN-specific thermal challenge is dynamic on-resistance ($R_{DS(on)}$) degradation, in which the effective on-resistance under switching conditions exceeds the static datasheet value due to charge trapping in the device epitaxial structure. Gill et al. [17] reviewed GaN HEMT dynamic on-resistance and field distribution effects, identifying current-collapse phenomena as a key reliability concern in high-voltage, high-frequency switching applications. Mitigation strategies including surface passivation, gate field plates, and p-GaN gate structures have been adopted in commercial enhancement-mode GaN devices to reduce dynamic $R_{DS(on)}$ to within 10-30% of static values under application-relevant conditions.

Despite substantial progress in individual topology and device-level studies, a systematic optimisation framework that jointly addresses switching frequency selection, dead-time management, ZVS range, EMI, and

thermal constraints for GaN-based EV fast-charging inverters across both 400 V and 800 V architectures remains lacking. Existing comparative studies between GaN and SiC typically focus on single topologies or single voltage classes, limiting their utility for system-level inverter selection. This work addresses these gaps by presenting a unified optimisation methodology and topology-selection framework.

## 3. Methodology

The reference inverter architecture examined in this work comprises two cascaded power conversion stages: a single-phase bridgeless totem-pole PFC rectifier as the AC-DC front-end, followed by a full-bridge LLC resonant converter as the isolated DC-DC stage. This two-stage architecture is representative of current best-practice for single-phase EV chargers in the 3.3-22 kW power range. The PFC stage converts 230 V AC grid input to a regulated 400 V DC bus, while the LLC stage provides galvanic isolation and regulates the output voltage across the 250-450 V battery voltage range typical of contemporary passenger EVs. Design targets are set as: peak system efficiency ≥ 97.5%, power density ≥ 3 kW/L, power factor ≥ 0.99, THD ≤ 5%, and compliance with CISPR 32 Class B conducted emission limits.

Switching frequency selection for GaN-based converters involves a trade-off between passive component size — which scales inversely with frequency — and switching losses, which scale proportionally. For the totem-pole PFC stage, the total power loss P_total at frequency f_s is approximated as:

P_total = P_cond + P_sw + P_core

where P_cond represents conduction loss (largely frequency-independent), P_sw represents switching loss (linear in f_s for hard-switching, near-zero for ZVS), and P_core represents magnetic core loss (scaling approximately as f_s^1.5-2 depending on core material). For GaN devices operating in CCM totem-pole PFC, P_sw is dominated by output capacitance (C_oss) charging and discharging energy rather than reverse-recovery loss. The energy stored in C_oss per switching event scales as $E_{oss} = \frac{1}{2} C_{oss} V_{ds}^2$, driving selection of devices with minimum C_oss for a given V_ds rating. Optimal switching frequency is found in the range 100-300 kHz for 6.6-22 kW PFC stages using 650 V GaN devices, balancing core loss in ferrite inductors against achievable power density.

Dead time t_d in the totem-pole PFC and LLC bridge legs must be sufficient to ensure complete discharge of the complementary switch's C_oss before gate-turn-on, achieving ZVS. The minimum dead time for ZVS is:

$t_{d,min} = 2 C_{oss} V_{dc} / I_{L,min}$

where V_dc is the DC bus voltage and I_L,min is the minimum instantaneous inductor current at the switching instant. For GaN devices with low C_oss (typically 60-150 pF for 650 V 25 mΩ class devices), t_d,min values of 20-80 ns are achievable, compared to 200-500 ns for equivalent SiC MOSFETs. Minimising dead time beyond t_d,min is critical because body diode (or third-quadrant) conduction during dead time incurs a forward voltage drop of 1.8-2.2 V in GaN devices — significantly higher than the 0.7-1.0 V of equivalent SiC body diodes — making dead-time management more important for GaN efficiency. An adaptive dead-time control scheme using high-speed gate-driver integrated circuits with ZVS detection feedback is implemented to dynamically adjust t_d across the operating range.

High switching frequencies in GaN converters generate conducted EMI across the 150 kHz-30 MHz range regulated by CISPR 32 and IEC 61851-21-1 for EV charging applications. The primary EMI sources in the totem-pole PFC are the common-mode (CM) and differential-mode (DM) currents driven by the high dv/dt at the switching node — typically 10-50 V/ns in GaN implementations, compared to 1-5 V/ns in Si IGBT designs. EMI filter design for GaN converters must address these elevated dv/dt values while minimising filter volume, which partially offsets the passive size reductions achieved through higher switching frequency.

A two-stage CM/DM EMI filter topology is implemented, with filter component values determined through impedance-mismatch methodology. The filter corner frequency is set to one decade below the switching frequency for the first-stage attenuation requirement, with the second stage providing rolloff in the 1-30 MHz range where radiated coupling becomes significant. Gate-drive slew-rate control — reducing the gate drive current to slow the dv/dt at the switching node — provides an additional degree of freedom for EMI-efficiency trade-off optimisation without external filter modification [3].

A lumped-parameter thermal model is constructed for each GaN switching device, comprising junction-to-case resistance $R_{\theta jc}$, case-to-heatsink resistance $R_{\theta cs}$ (incorporating thermal interface material), and heatsink-to-ambient resistance $R_{\theta ha}$. Junction temperature $T_j$ is computed as:

$$T_j = T_{amb} + P_{loss} \times (R_{\theta jc} + R_{\theta cs} + R_{\theta ha})$$

GaN HEMTs have a lower maximum junction temperature rating (typically 150°C) than SiC MOSFETs (175°C) and a lower thermal conductivity substrate when grown on Si (vs. SiC native substrate). For the target 6.6 kW inverter, forced-air cooling with a heatsink of $R_{\theta ha} = 0.5$°C/W is specified, constraining maximum device power dissipation to approximately 25 W per device at a 40°C ambient and 20 W thermal design margin. This thermal budget is satisfied by the selected 650 V / 25 mΩ p-GaN gate enhancement-mode HEMT operating at 300 kHz in the PFC stage with ZVS operation ensuring near-zero switching loss.

## 4. Results and Discussion

A comparative efficiency evaluation across GaN, SiC, and Si device technologies is conducted for the 6.6 kW totem-pole PFC stage at 300 kHz switching frequency and unity power factor. GaN-based implementation achieves a peak efficiency of 98.7%, compared to 98.2% for SiC and 96.4% for Si MOSFET implementations at the same switching frequency. The efficiency advantage of GaN is most pronounced in the 20-80% load range, where switching losses dominate over conduction losses, and GaN's negligible reverse-recovery and low $C_{oss}$ confer a decisive advantage [3]. At very light loads (below 10%), the elevated body-diode forward voltage of GaN devices partially erodes the efficiency advantage, motivating adaptive dead-time strategies that minimise diode conduction intervals.

For the LLC resonant DC-DC stage at 500 kHz, GaN achieves 98.1% peak efficiency compared to 97.6% for SiC. The two-stage cascade achieves a system-level peak efficiency of 96.9% for GaN, consistent with the best reported results for comparable power class from the recent literature [14]. Power density of the GaN inverter prototype is 3.2 kW/L, representing a 45% improvement over the Si baseline and a 22% improvement over the SiC implementation at the same power level, driven primarily by passive component volume reductions enabled by higher switching frequency.

System efficiency and power density are evaluated across switching frequencies from 50 kHz to 500 kHz for the PFC stage with GaN devices. Peak system efficiency is observed at 200-300 kHz, where the trade-off between switching loss and core loss is optimised for the selected ferrite core material (3C96 grade). Above 300 kHz, core losses in the PFC inductors begin to dominate, eroding efficiency despite reduced winding copper losses. Power density increases monotonically with frequency up to approximately 400 kHz, above which EMI filter volume grows to offset passive size reductions, resulting in an optimal power density at 350-400 kHz. This frequency range also corresponds to the minimum weighted total cost function combining efficiency and density objectives for the target EV fast-charging application.

ZVS operation of the LLC resonant stage is maintained across the full battery voltage range (250-450 V) through adaptive frequency modulation with a variable frequency range of 380-560 kHz centred on a resonant frequency of 470 kHz. Dead-time sensitivity analysis reveals that efficiency at 25% load degrades by 0.8% per 50 ns of excess dead time, confirming the importance of adaptive dead-time control for GaN LLC implementations [13]. With the implemented ZVS detection feedback scheme, average dead time is reduced from a fixed 80 ns to

an adaptive range of 22-65 ns depending on operating point, recovering 0.6% efficiency at the 25% load point relative to fixed dead-time operation.

Conducted EMI measurements at the two-stage inverter input confirm compliance with CISPR 32 Class B limits with a two-stage CM/DM filter occupying 0.31 L — representing 9.7% of the total inverter volume. Gate-drive slew-rate reduction from maximum (dv/dt = 35 V/ns) to controlled (dv/dt = 12 V/ns) reduces peak conducted EMI by 8 dB at the first switching harmonic with a measured efficiency penalty of 0.15% — a favourable trade-off for applications with stringent EMI requirements. The EMI filter volume requirement increases by 18% when the switching frequency is raised from 200 kHz to 400 kHz at fixed attenuation target, partially offsetting the passive volume reduction achieved in the power stage.

Thermal measurements on the prototype GaN HEMT devices under rated operating conditions confirm maximum junction temperatures of 118°C — within the 150°C rated maximum — with a thermal margin of 32°C providing derating headroom for elevated ambient temperatures. Dynamic R_DS(on) characterisation under application-representative switching conditions reveals a 22% increase relative to static datasheet values at 400 V bus voltage, consistent with published data for p-GaN gate enhancement-mode devices [17]. This R_DS(on) increase is accounted for in the loss model through a dynamic correction factor, and does not materially affect compliance with the ≥ 97.5% efficiency target. The thermal model predictions show good agreement with measured junction temperatures, with maximum deviation of 4°C across the operating range.

## 5. Discussion

The optimisation results support a topology-selection framework for GaN-based EV fast-charging inverters that distinguishes between 400 V and 800 V battery architectures. For 400 V bus systems, 650 V GaN devices in two-level totem-pole PFC and full-bridge LLC configurations represent the optimal balance of efficiency, power density, and implementation cost. The switching frequency range of 200-300 kHz for the PFC stage and 400-500 kHz for the LLC stage, with adaptive dead-time control, consistently delivers system efficiencies above 97% across the 20-100% load range. For 800 V bus architectures, direct application of 650 V GaN devices requires three-level converter topologies (Vienna rectifier or T-type) that halve the device voltage stress, or series-stacked two-level implementations with active voltage sharing. SiC MOSFETs with 1200 V ratings retain an advantage for direct two-level 800 V implementations due to higher voltage headroom and more mature gate-driver ecosystems [7].

GaN HEMT gate-driver design presents unique challenges relative to SiC MOSFET practice. Enhancement-mode p-GaN gate devices require gate voltages of +6 V (on) and 0 V (off), compared to the +15 V / -5 V range standard for SiC. While the lower gate voltage swing simplifies bootstrap supply design, it reduces the noise margin against spurious turn-on caused by Miller coupling — a concern at the high dv/dt values characteristic of GaN switching. Kelvin-source gate drive connections, minimising common-source inductance, are mandatory for stable GaN HEMT operation above 200 kHz. Integrated GaN power stage and gate-driver ICs, which co-package the gate driver with the power HEMT to eliminate package-level inductances, have substantially reduced the gate-driver design burden and represent the recommended approach for new designs targeting frequencies above 300 kHz [8].

GaN HEMT reliability in automotive and charging applications has been an area of active investigation. The primary device-level failure mechanisms include gate dielectric degradation under repetitive switching stress, hot-electron trapping leading to threshold voltage shift, and time-dependent breakdown of the AlGaN barrier under high electric field. Commercial p-GaN gate devices from major manufacturers have achieved AEC-Q101 automotive qualification, providing baseline reliability assurance for OBC applications. However, system-level reliability data from EV fast-charging field deployments remain limited, and accelerated life testing protocols specifically tailored to GaN HEMT failure mechanisms under representative EV charge-cycle profiles are still being developed by standardisation bodies. Lifetime prediction under real EV drive cycle conditions, integrating both thermal cycling and electrical stress, represents a priority research area [3].

The cost of GaN devices has declined substantially as manufacturing volumes have scaled, driven primarily by adoption in consumer USB-C fast chargers. 650 V GaN FETs are now commercially available at price points within 1.5-2× the cost of equivalent SiC devices and 3-4× the cost of Si MOSFETs of similar on-resistance. The system-level cost comparison is more favourable for GaN than the device-level comparison suggests, as reduced passive component volume and elimination of bulky heatsink assemblies in high-efficiency GaN designs partially offset the device cost premium. For EV fast-charging applications where power density commands a premium — particularly for off-board DC chargers that must fit within limited enclosure footprints — GaN represents a compelling solution at current pricing, with cost parity with SiC projected within the 2025-2027 timeframe as GaN-on-Si manufacturing scales to 200 mm wafer processes [2].

## 6. Conclusions

This paper has presented a systematic optimisation analysis of GaN-based two-stage inverter architectures for EV fast-charging applications, encompassing totem-pole PFC and LLC resonant converter stages. The principal findings are: (i) GaN-based implementations achieve system-level peak efficiencies of 96.9% and power densities of 3.2 kW/L at the 6.6 kW power level, representing gains of 45% in power density relative to Si baselines; (ii) optimal switching frequency for the PFC stage lies in the 200-300 kHz range, balancing core loss and passive size objectives; (iii) adaptive dead-time control with ZVS detection feedback recovers 0.6% efficiency at light load relative to fixed dead-time schemes; (iv) dynamic $R_{DS(on)}$ degradation of 22% relative to static values is observed and must be incorporated in accurate loss models; and (v) a topology-selection framework distinguishes 650 V GaN two-level topologies as optimal for 400 V bus architectures, while 800 V systems require three-level GaN or SiC-based solutions pending availability of higher-voltage GaN devices.

Future research priorities include: the development of GaN-specific accelerated life testing protocols for EV charging duty cycles; investigation of MHz-range switching operation with planar integrated magnetics to further advance power density; data-driven reliability evaluation integrating field deployment data; and extension of the optimisation framework to multi-port charger architectures supporting simultaneous grid, vehicle, and energy-storage interactions within vehicle-to-grid (V2G) enabled charging infrastructure.

## REFERENCES

[1] G. Iannaccone, C. Sbrana, I. Morelli, and S. Strangio, "Power electronics based on wide-bandgap semiconductors: Opportunities and challenges," IEEE Access, vol. 9, pp. 139446–139456, 2021.

[2] M. Buffolo et al., "Review and outlook on GaN and SiC power devices: Industrial state-of-the-art, applications, and perspectives," IEEE Trans. Electron Devices, vol. 71, no. 3, pp. 1344–1355, Mar. 2024.

[3] N. Karaoglu et al., "GaN electric vehicle systems—A comparative review," Energies, vol. 18, no. 22, pp. 6020, Nov. 2025.

[4] G. A. Mudiyanselage, N. Keshmiri, and A. Emadi, "A review of DC-DC resonant converter topologies and control techniques for electric vehicle applications," IEEE Open J. Power Electron., vol. 4, pp. 945–964, 2023.

[5] R. Coppola, F. Nappi, and M. Paparo, "A comprehensive review of GaN-based bi-directional on-board charger topologies and modulation methods," Energies, vol. 16, no. 8, pp. 3433, Apr. 2023.

[6] K. J. Chen, O. Häberlen, A. Lidow, C. Lin Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si power technology: Devices and applications," IEEE Trans. Electron Devices, vol. 64, no. 3, pp. 779–795, Mar. 2017.

[7] V. Smet et al., "Power semiconductor considerations for xEV applications," in CS MANTECH Conf., pp. 1–4, Orlando, FL, 2023.

[8] G. Iannaccone, C. Sbrana, I. Morelli, and S. Strangio, "Power electronics based on wide-bandgap semiconductors: Opportunities and challenges," IEEE Access, vol. 9, pp. 139446–139456, 2021.

[9] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," IEEE J. Emerg. Sel. Top. Power Electron., vol. 4, no. 3, pp. 799–807, Sep. 2016.

[10] J. W. M. Soares and A. A. Badin, "High-efficiency interleaved totem-pole PFC converter with voltage follower characteristics," IEEE J. Emerg. Sel. Top. Power Electron., vol. 11, no. 2, pp. 1879–1887, Apr. 2023.

[11] S. Kamarajugadda and S. Kadiyala, "Design optimization of a 7.2 kW totem-pole power factor correction converter for onboard electric vehicle charger," Semantic Scholar, 2023.

[12] G. A. Mudiyanselage, N. Keshmiri, and A. Emadi, "A review of DC-DC resonant converter topologies and control techniques for electric vehicle applications," IEEE Open J. Power Electron., vol. 4, pp. 945–964, 2023.

[13] Y. Zhang, W. Xu, Y. Xie, T. Liu, Z. Wu, C. Chen, Y. Kang, and H. Peng, "Analysis of dead-time energy loss in GaN-based TCM converters with an improved GaN HEMT model," IEEE Trans. Power Electron., vol. 38, no. 2, pp. 1806–1818, Feb. 2023.

[14] A. Elezab, O. Zayed, A. Abuelnaga, and M. Narimani, "High efficiency LLC resonant converter with wide output range of 200–1000 V for DC-connected EVs ultra-fast charging stations," IEEE Access, vol. 11, pp. 33037–33048, 2023.

[15] M. Malakoutian, X. Zheng, M. Kuball, and S. Chowdhury, "Thermal management in GaN-devices for increased power density," in CS MANTECH Conf., pp. 1–4, Orlando, FL, 2023.

[16] D. Lumbreras, M. Vilella, J. Zaragoza, N. Berbel, J. Jordà, and A. Collado, "Effect of the heat dissipation system on hard-switching GaN-based power converters for energy conversion," Energies, vol. 14, no. 19, pp. 6287, Oct. 2021.

[17] L. Gill, S. DasGupta, J. C. Neely, R. J. Kaplar, and A. J. Michaels, "A review of GaN HEMT dynamic on-resistance and dynamic stress effects on field distribution," IEEE Trans. Power Electron., vol. 39, no. 1, pp. 517–537, Jan. 2024.